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10/790,852	03/02/2004	Karsten Wieczorek	2000.110600	3105

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EXAMINER	
ORTIZ, EDGARDO	
ART UNIT	**PAPER NUMBER**
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,852	WIECZOREK ET AL.	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 21-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 21-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-4, 9-15, 21-23 and 25-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Chan et al. (U.S. Patent No. 6,252,277). With regard to Claim 1, Chan discloses a method of forming a field effect transistor, the method comprising:

forming an implantation mask (37) over a crystalline semiconductor region (30) (figure 4C);

forming drain and source regions (39) adjacent said implantation mask (37) (figure 4E), said drain and source regions (39) each having a top surface located above a top surface of said crystalline semiconductor region (30) (figure 4E);

removing said implantation mask (37) to expose a top surface area of said crystalline semiconductor region (30);

forming a gate insulation layer (44) on said exposed surface area (column 5, lines 57-59);

forming a gate electrode (47), out of polysilicon layer (46), on said gate insulation layer (44); and

doping said gate electrode (column 5, lines 61-67 and column 6, lines 1-7).

With regard to Claim 2, Chan discloses forming a gate electrode (47) including depositing a gate electrode material (46) comprising polysilicon (column 5, lines 61-63) above a gate insulation layer (44) and removing excess material of said gate electrode material (46) to form the gate electrode (47) (column 6, lines 8-9 and figure 4I).

With regard to Claim 3, Chan discloses a lateral size of the implantation mask (37) that is greater than a design value of a gate length of the gate electrode (47), as clearly seen on figures 4B, 4F and 4I, wherein the implantation mask (37) occupies a lateral size that is larger than that which is occupied by gate electrode (47) as part of the final structure disclosed by the reference.

With regard to Claim 4, Chan discloses forming drain and source regions (39) by epitaxially-growing (column 5, lines 7-17) a crystalline semiconductor layer adjacent to an implantation mask (37).

With regard to Claim 9, Chan discloses forming sidewall spacers (35) on sidewalls of the drain and source regions (column 5, lines 10-13) that are exposed by removing an implantation mask (37).

With regard to Claim 10, Chan discloses a width of sidewalls spacers (35) controlled on the basis of target length (figure 4B) for a gate electrode (47).

With regard to Claim 11, Chan discloses an implantation mask (37) that is removed by an isotropic-etch process (column 5, lines 51-54).

With regard to Claim 12, Chan discloses removing an excess material (46) to form a gate electrode (47), by chemical-mechanical polishing (column 6, lines 8-9).

With regard to Claim 13, Chan discloses removing an excess material (46) to form a gate electrode (47), by an etch-process (column 6, lines 9-10).

With regard to Claim 14, Chan discloses removing an excess material (46) to form a gate electrode (47), by chemical-mechanical polishing (column 6, lines 8-9) and an etch-process (column 6, lines 9-10).

With regard to Claim 15, Chan discloses forming metal/semiconductor compound regions (48A, 48B) (column 6, lines 29-39) on the gate electrode (47) and drain and source regions (39).

With regard to Claim 21, Chan discloses doping of the gate electrode (47) that is performed on the basis of process parameters selected to restrict dopant-penetration of the gate insulation layer (column 5, lines 57-67 and column 6, lines 1-3).

With regard to Claim 22, Chan discloses a field-effect transistor (column, lines 4-6), comprising:

a substrate (30) having formed thereon a semiconductor region having a top surface; a drain region (39) formed on said top surface of said semiconductor region and extending along a lateral direction and a height direction (figure 4E); a source region (39) formed on said top surface of said semiconductor region and extending along a lateral direction and a height direction (figure 4E); a gate electrode (47)) formed above said top surface of said semiconductor region and extending along said lateral direction and said height direction said gate electrode (47) laterally located between said drain and source regions (39) and separated from said top semiconductor region by a gate insulation layer (44), said drain and source regions (39) extending along said height direction at least to an upper surface of said gate electrode (47) (figure 4E).

With regard to Claim 23, Chan discloses a gate electrode (47) that is partially-comprised of a doped semiconductor material (column 5, lines 67-68 and column 6, lines 1-3); whereby a peak concentration of dopants in said gate electrode is less than a peak concentration of dopants in said drain and source regions (39), since said drain and source regions (39) are heavily-doped (column 5, lines 13-15).

With regard to Claim 25, Chan discloses a method of forming a field effect transistor (column, lines 4-6), the method comprising:

forming a recess (136) in a semiconductor layer (30), said recess having a bottom surface; forming an implantation mask (137) in at least said recess (136);

forming drain and source regions (139) by performing at least one ion implantation to implant ions (arsenic) into said semiconductor layer (30) adjacent said implantation mask, wherein said implantation mask (137) substantially prevents ions from penetrating said bottom surface of said recess (136);

removing said implantation mask to expose said bottom surface of said recess (136) (column 8, lines 57-60);

forming a gate insulation layer (144) on said exposed surface area (column 8, lines 64-67);

forming a gate electrode (147), out of polysilicon layer (146), on said gate insulation layer (144) (column 9, lines 1-25); and

doping said gate electrode (column 9, lines 4-14).

With regard to Claim 26, Chan discloses forming a gate electrode (47) including depositing a gate electrode material comprising polysilicon (column 5, lines 61-63) above a gate insulation layer (44) and removing excess material of said gate electrode to form the gate electrode (column 6, lines 8-12 and figure 4I).

With regard to Claim 27, Chan discloses forming sidewall spacers (135), prior to forming the gate insulation layer (144), on sidewalls of the recess (136) that are exposed by removing an implantation mask (137).

With regard to Claim 28, Chan discloses a width of sidewalls spacers (135) controlled on the basis of target length (figure 6B) for a gate electrode (147).

With regard to Claim 29, Chan discloses an implantation mask (37) that is removed by an isotropic-etch process (column 5, lines 51-54).

With regard to Claim 30, Chan discloses forming metal/semiconductor compound regions (148A, 148B) (column 6, lines 29-39) on the gate electrode (47) and drain and source regions (39).

With regard to Claim 31, Chan discloses a lateral dimension of a recess (136) that is greater than a target length of a gate electrode (47), (figures 4B and 4I).

With regard to Claim 32, Chan discloses a recess (136) formed by anisotropically etching the semiconductor layer (30) (column 7, lines 44-50).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (U.S. Patent No. 6,252,277) in view of Applicant's admitted prior art as disclosed on pages 1-8

and figures 1a-1d of the instant application. With regard to Claim 5, Chan essentially discloses the claimed invention but fails to disclose the claimed steps of a first implantation sequence for drain and source regions is performed prior to epitaxially-growing the semiconductor layer and a second implantation sequence for forming said drain and source regions is performed after epitaxially-growing the semiconductor layer. However, Applicant's admitted prior art discloses a process for forming a transistor which includes the steps of a first implantation sequence for drain and source regions (108) (see page 5, lines 21-24 of the instant application) that is performed prior to epitaxially-growing silicon regions (111) (see page 7, lines 11-12 of the instant application), wherein the epitaxially-growing silicon regions (111) may be grown prior to or after a final implantation cycle for forming the drain and source regions (108) (see page 7, lines 13-15 of the instant application). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the process as disclosed by Chan to include the claimed steps of a first implantation sequence for drain and source regions is performed prior to epitaxially growing the semiconductor layer and a second implantation sequence for forming said drain and source regions is performed after epitaxially growing the semiconductor layer, as clearly suggested by Applicant's admitted prior art, in order to reduce contact resistance to the drain and source regions (see page 7, lines 1-9 of the instant application).

With regard to Claim 6, a further difference between the claimed invention and Chan is the claimed step of an anneal process to activate the dopants. However, Applicant's admitted prior art discloses a process for forming a transistor, which includes the step of using an anneal

process to activate dopants on drain and source regions (108) (see page 5, lines 21-24 and page 6, lines 3-5 of the instant application). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the process as disclosed by Chan to include the claimed step of an anneal process to activate the dopants, as clearly suggested by Applicant's admitted prior art, in order to activate dopants and re-crystallize portions of drain and source regions that are damaged during implantation sequences (see page 6, lines 3-5 of the instant application).

With regard to Claim 7, a further difference between the claimed invention and Chan is the claimed anneal process controlled on the basis of a desired channel length defined by a lateral distance of the drain region and the source region. However, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the process as disclosed by Chan to include the claimed anneal process controlled on the basis of a desired channel length defined by a lateral distance of the drain region and the source region, in order to optimize the channel-length and thus reduce problems associated with a channel region, namely leakage current.

With regard to Claim 8, a further difference between the claimed invention and Chan is the claimed step of an anneal cycle performed after said first implantation sequence and prior to said second implantation sequence, said first anneal cycle being configured to substantially completely re-crystallize amorphized portions in said semiconductor region. However, Applicant's admitted prior art discloses a process for forming a transistor, which includes the

step of using an anneal process to activate dopants and re-crystallize portions of drain and source regions (108) that are damaged by previous implantation sequences (see page 5, lines 21-24 and page 6, lines 3-5 of the instant application). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the process as disclosed by Chan to include the claimed step of an anneal process to activate the dopants, as clearly suggested by Applicant's admitted prior art, in order to activate dopants and re-crystallize portions of drain and source regions that are damaged during implantation sequences (see page 6, lines 3-5 of the instant application).

3. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (U.S. Patent No. 6,252,277) in view of Gardner (U.S. Patent No. 6,355,955). With regard to Claim 24, Chan essentially discloses the claimed invention but fails to disclose the claimed semiconductor region formed on an insulating layer and having an extension in the height direction in the range of approximately 5-50 nm.

However, Gardner discloses that the height of a semiconductor layer can be modified as desired (column 12, lines 36-54). Therefore it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the method as disclosed by Chan to include the claimed height, in order to minimize diffusion of impurities into the channel region (column 12, lines 50-54). Additionally, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. Regarding the claimed insulating layer, it would have been

obvious to someone with ordinary skill in the art, at the time of the invention, to modify the method as disclosed by Chan to include a semiconductor region formed on an insulating layer, in order to provide an insulating layer for semiconductor device such as a thin-film transistor (TFT).

Response to Arguments

4. Applicant's arguments filed March 28, 2005 have been fully considered, but are not deemed persuasive. Applicant first argues that "*Since the implantation mask identified by the Examiner does not exist at the time the drain and source regions are formed, Chan, by definition, cannot disclose forming a drain region and a source region adjacent the implantation mask as now set forth in amended independent claim 1.*" However, the examiner disagrees and notes that as clearly stated in the rejection, Chan discloses the step forming drain and source regions (39) by epitaxially-growing (column 5, lines 7-17) a crystalline semiconductor layer adjacent to an implantation mask (37), as illustrated in figure 4E, which shows **both** source and drain regions (39) and implantation mask (37) during the step described above.

Applicant further argues that "*independent claim 1 has been amended to recite that it is a top surface of the crystalline semiconductor region that is exposed when the implantation mask is removed and that the gate insulation is formed on the exposed surface area of the top surface of the crystalline semiconductor region*", in order to distinguish the claimed invention form that taught by Chan. However, the claimed invention does not patentably distinguish from Chan, since the reference discloses a top surface, namely the portion of crystalline layer (30) that is exposed, having a gate oxide layer (44) formed on said top surface.

Applicant also argues that "*independent claim 22 has been amended to recite that the drain and source regions are formed on the top surface of the semiconductor region, that the gate electrode is formed above the top surface of the semiconductor region and that the gate electrode is separated from the top surface of the semiconductor region by a gate insulation layer. As thus amended, it is respectfully submitted that Chan does not disclose or suggest the invention set forth in amended independent claim 22.*" The examiner refers to the rejection of claim 22, which states that Chan discloses a drain region (39) formed on said top surface of semiconductor region (30) and extending along a lateral direction and a height direction (figure 4E); a source region (39)) formed on said top surface of said semiconductor region and extending along a lateral direction and a height direction (figure 4E); a gate electrode (47)) formed above said top surface of said semiconductor region and extending along said lateral direction and said height direction said gate electrode (47) laterally located between said drain and source regions (39) and separated from said top semiconductor region by a gate insulation layer (44). Thus, claim 22 clearly does not patentably distinguish from Chan.

Lastly, Applicant argues regarding new claim 25 that "*the prior art of record neither anticipates nor renders obvious the invention defined by new independent claim 25. Accordingly, it is respectfully submitted that new claims 25-32 are likewise allowable over the art of record.*" The examiner also refers to the rejection and notes that Chan discloses all of the claimed limitations and explicitly shown in the body of the rejection.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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